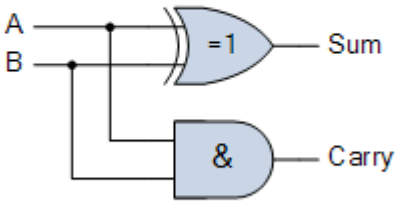
EEL 3712L LOGIC DESIGN I LAB

Practice for Final – Summer, 2019

Instructor: Abdullah Aydeger

1. Design a *half* adder/subtract Circuit with XOR, AND and Inverter (whichever needed) gates.

Answer:

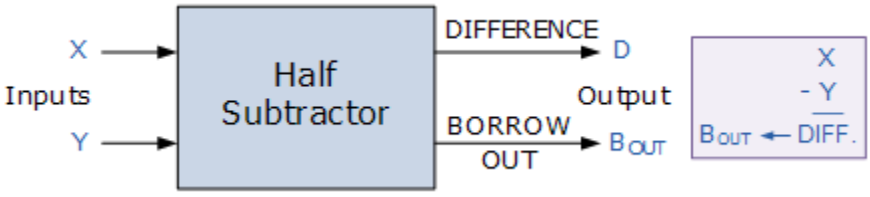
Symbol	Truth Table			
	B	A	SUM	CARRY
	0	0	0	0
	0	1	1	0
	1	0	1	0
	1	1	0	1

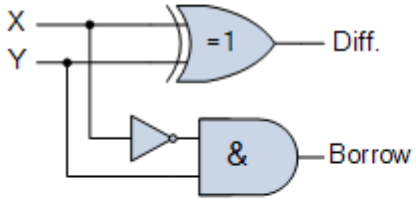
SUM = A XOR B = A ⊕ B

CARRY = A AND B = A.B

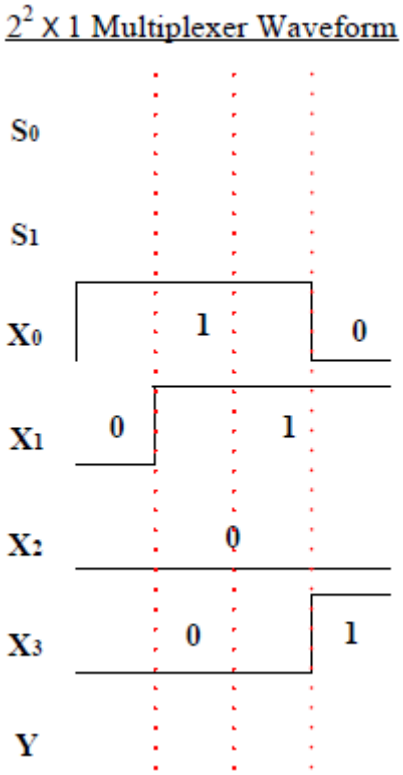
Half Subtractor with Borrow-out

D = X XOR Y = X ⊕ Y B = not-X AND Y



Symbol	Truth Table			
	Y	X	DIFFERENCE	BORROW
	0	0	0	0
	0	1	1	0
	1	0	1	1
	1	1	0	0

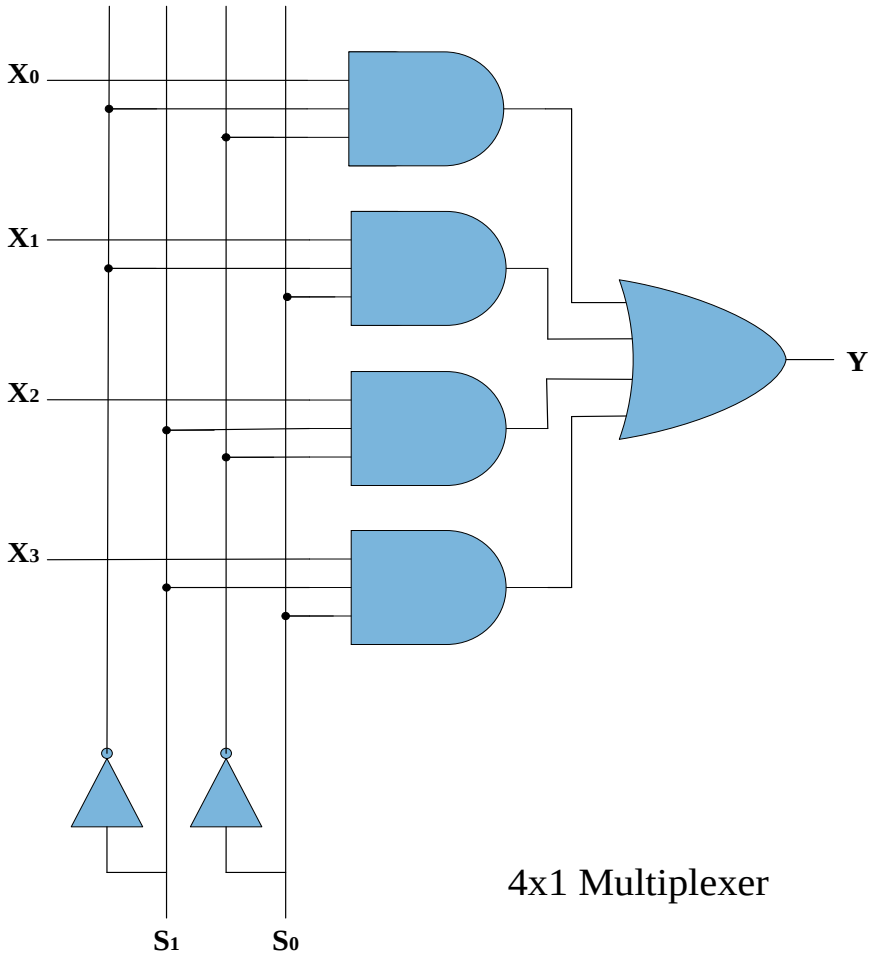
2. Design a 4-to-1 Multiplexer with gates and invertors.
    a. Make the Truth table and the equation, you may use De Morgan' Law convert into universal gates(NAND and NOR) for the diagram
    b. Draw the diagram
    c. Complete the waveform
    d. Design Half-adder using this MUX(es).



Answer: $Y=S'_1 \cdot S'_0 \cdot X_0 + S'_1 \cdot S_0 \cdot X_1 + S_1 \cdot S'_0 \cdot X_2 + S_1 \cdot S_0 \cdot X_3$

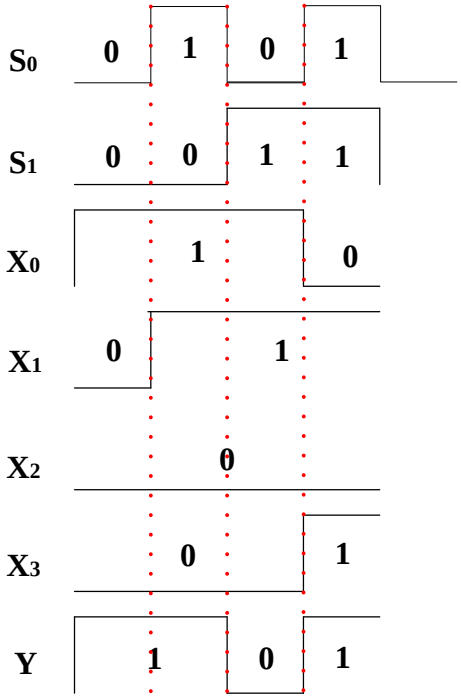
4 X 1 Multiplexer Truth Table

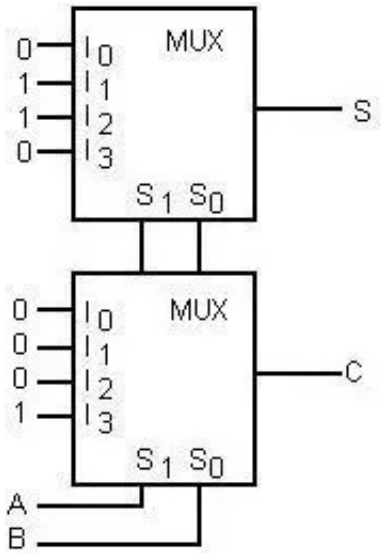
Inputs						Output
S_0	S_1	X_0	X_1	X_2	X_3	Y
0	0	0	x	x	x	0
0	0	1	x	x	x	1
1	0	x	0	x	x	0
1	0	x	1	x	x	1
0	1	x	x	0	x	0
0	1	x	x	1	x	1
1	1	x	x	x	0	0
1	1	x	x	x	1	1



4x1 Multiplexer

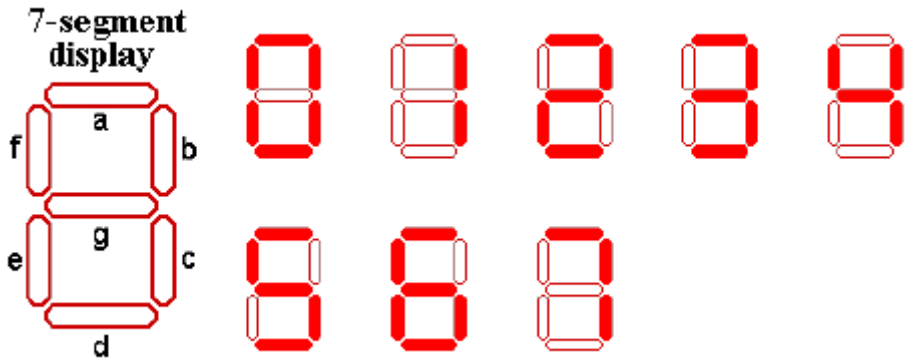
2^2 x 1 Multiplxer Wave Form





S = sum C =carry-out A and B are inputs (A+B)

3. 7-Segment Octal Number (from 0 to 7) display driver could display the octal number given by the three inputs I2I1I0 using a 7-Segment LED device as shown in Fig 1. The truth table for this circuit is in Tab. 4, please fill in it and write the Minterms of each segment of LED display for this driver.



Binary-coded Octal to 7-Segment Display Decoder Truth Table

Decoder Input			Decoder Outputs (Octal#)	Inputs of Common Cathode 7-Segment LED Display						
I2	I1	I0		a	b	c	d	e	f	g

Write Minterms of:

a= Σ (0, 2, 3, 5, 6, 7)

b= e=

c= f=

d= g=

Answer:

Binary-coded Octal to 7-Segment Display Decoder Truth Table

Decoder Input			Decoder Outputs (Octal#)	Inputs of Common Cathode 7-Segment LED Display						
I_2	I_1	I_0		a	b	c	d	e	f	g
0	0	0	**0**	1	1	1	1	1	1	0
0	0	1	**1**	0	1	1	0	0	0	0
0	1	0	**2**	1	1	0	1	1	0	1
0	1	1	**3**	1	1	1	1	0	0	1
1	0	0	**4**	0	1	1	0	0	1	1
1	0	1	**5**	1	0	1	1	0	1	1
1	1	0	**6**	1	0	1	1	1	1	1
1	1	1	**7**	1	1	1	0	0	0	0

a= $\sum$ (0, 2, 3, 5, 6, 7)

b= $\sum$ (0, 1, 2, 3, 4, 7)

c=$\sum$ (0, 1, 3, 4, 5, 6, 7)

d=$\sum$ (0, 2, 3, 5, 6)

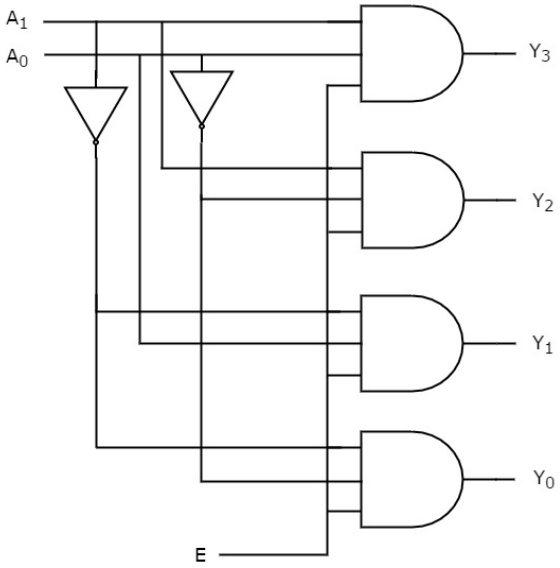
e=$\sum$ (0, 2, 6)

f=$\sum$ (0, 4, 5, 6)

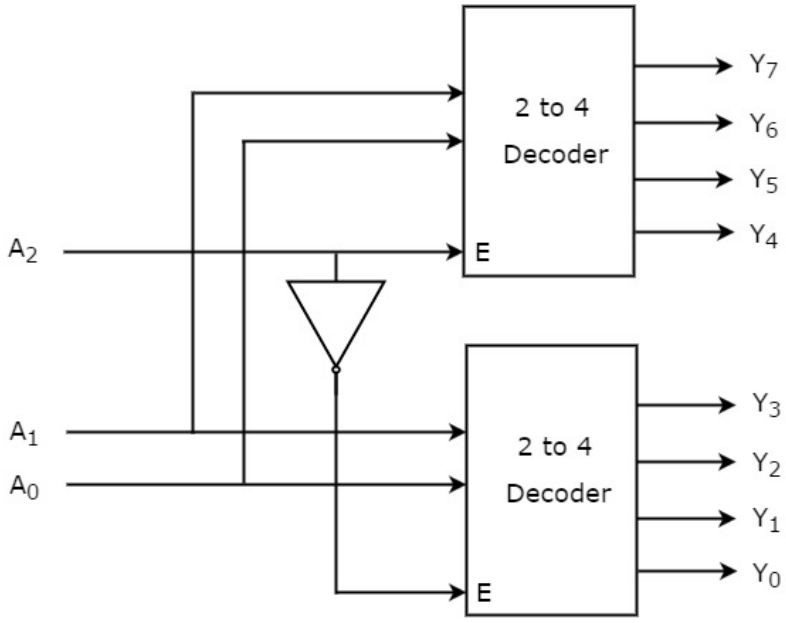
g=$\sum$ (2, 3, 4, 5, 6)

4. Design **Active-High** Output 2 to 4 Binary Decoder using AND gates. Consider Enable input for your design. Show the truth table. By using this decoder, design 3 to 8 decoder.

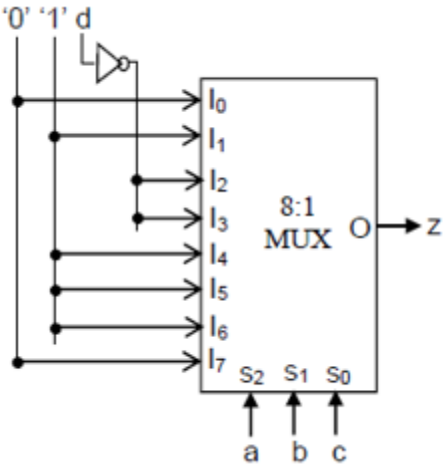
Answer:



Enable	Inputs		Outputs			
E	**A_1**	**A_0**	**Y_3**	**Y_2**	**Y_1**	**Y_0**
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0



5. (a) Construct truth table of the schematic.
   (b) Write the expression (equation) of Z = f(a,b,c,d).
   (c) Design and draw same function using 4:16 decoder.



Answer:

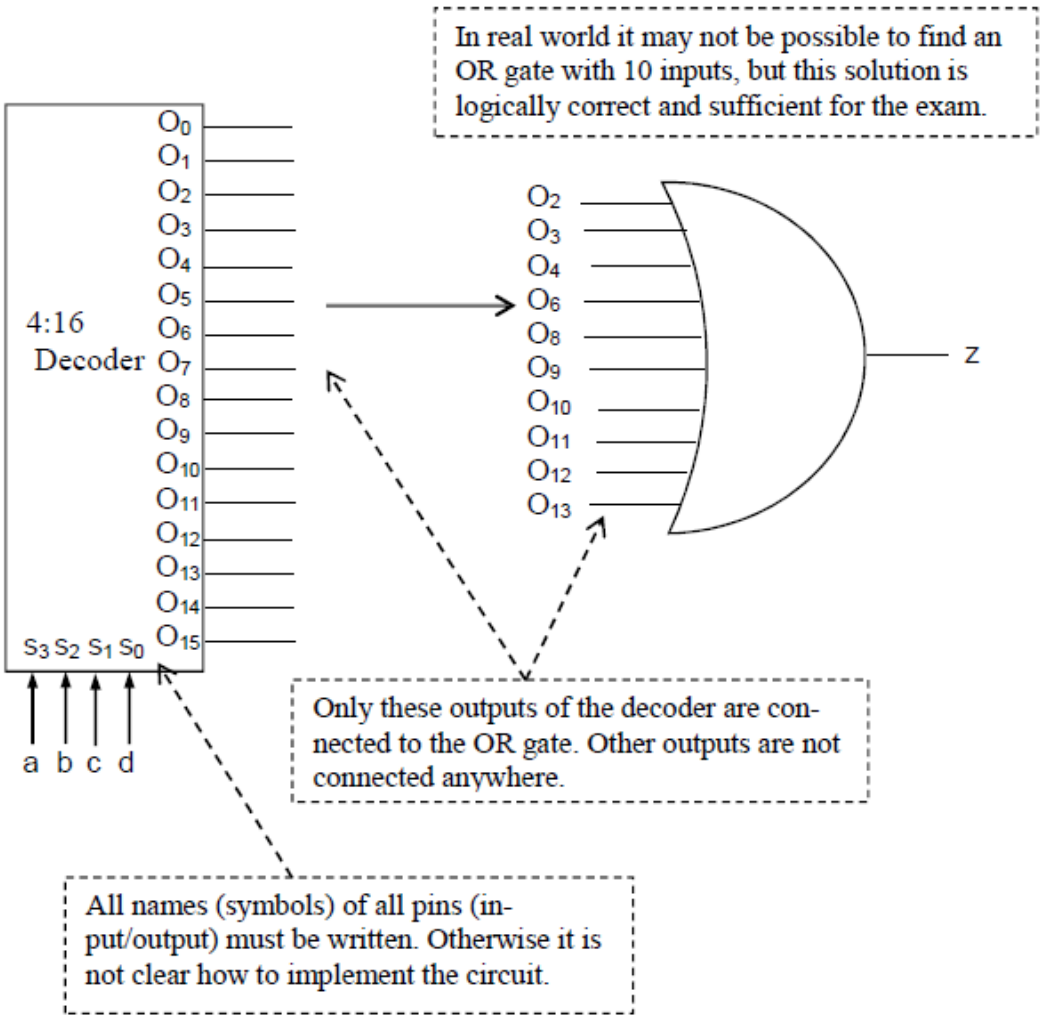
Truth table:

a b c d	z
0 0 0 0	0
0 0 0 1	0
0 0 1 0	1
0 0 1 1	1
0 1 0 0	1
0 1 0 1	0
0 1 1 0	1
0 1 1 1	0
1 0 0 0	1
1 0 0 1	1
1 0 1 0	1
1 0 1 1	1
1 1 0 0	1
1 1 0 1	1
1 1 1 0	0
1 1 1 1	0

z= a'b'cd'+ a'b'cd + a'bc'd'+ a'bcd'+ ab'c'd'+ ab'c'd + ab'cd' + ab'cd
+ abc'd'+ abc'd

<u>Remember that</u> a'b'c'd' + a'b'c'd = a'b'c'(d' + d) = a'b'c'

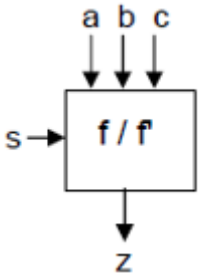
c.



6. Write the truth table of following function and then design the schematic using MUX(es) and 2 inverter gates.

   If s0 = 0 then z = f(a,b,c) = a'b + bc + b'c'

   If s=1 then z = f'(a,b,c)



Answer:

a	b	c	f(S=0)	
0	0	0	1	c'
0	0	1	0	
0	1	0	1	1
0	1	1	1	
1	0	0	1	c'
1	0	1	0	
1	1	0	0	c
1	1	1	1